2812

Docket No.: GR 99 P 1679

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By: _____ Date: July 23, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Gerald Deboy et al.
Applic. No.	:	10/033,227
Filed	:	October 22, 2001
Title	:	Semiconductor Component
Art Unit	:	2812

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 4,811,075 (Eklund), dated March 7, 1989.

United States Patent No. 5,170,241 (Yoshimura et al.), dated December 8, 1992;

United States Patent No. 5,285,369 (Balakrishnan), dated February 8, 1994;

United States Patent No. 5,296,725 (Nandakumar et al.), dated March 22, 1994;

United States Patent No. 5,313,082 (Eklund), dated May 17, 1994;

German Published, Non-Prosecuted Patent Application DE 44 29 284 A1 (Sack et al.), dated February 22, 1996, semiconductor component with two monolithic integrated circuits and a buried structured circuit area;

European Patent Application EP 0 585 788 A1 (Balakrishnan), dated March 9, 1994;

Japanese Patent Abstract JP 03 155 167 A (Shigeta et al.), dated July 3, 1991;

G. Deboy et al.: "A new generation of high voltage MOSFETs breaks the limit line of silicon", *IEDM 98, pp. 683-685, XP-000859463.*

International Search Report dated August 28, 2000;

International Preliminary Examination Report dated January 26, 2001.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

For Applicants

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FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
GR 99 P 1679	10/033,227

Applicant: Gerald Deboy et al.

Filing Date	Group Art Unit
October 22, 2001	2812

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A	4,811,075	03/07/89	Eklund			
	B	5,170,241	12/08/92	Yoshimura et al.			
	C	5,285,369	02/08/94	Balakrishnan			
	D	5,296,725	03/22/94	Nandakumar et al.			
	E	5,313,082	05/17/94	Eklund			
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	44 29 284 A1	02/22/96	Germany				X
	K	0 585 788 A1	03/09/94	Europe			X	
	L	03 155 167 A	07/03/91	Japan			X	
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	G. Deboy et al.: "A new generation of high voltage MOSFETs breaks the limit line of silicon", *IEDM 98, pp. 683-685, XP-000859463*
	P	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.